REMARKS

Claims 1-13 and 17-22 are pending. Claims 8 and 21 have been amended.

Claim 21 stands rejected under 35 U.S.C. § 112, first paragraph on the basis of non-compliance with the written description requirement. This rejection is respectfully traversed. Claim 21 has been amended for consistency with the specification. Reference to drivers 300, 302, shown in FIG. 3, is made on page 5, lines 11-14. Reference to SRAM 304, also shown in FIG. 3, is made on page 5, lines 15-16. The subject matter of claim 21 is described in the specification in such a way as to reasonably convey to one of ordinary skill in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Withdrawal of this rejection respectfully is requested.

Claims 1-4, 9-11, 13, and 17-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,834,782 to Schick et al. in view of U.S. Pat. No. 6,396,539 to Heller et al. Applicants respectfully request reconsideration of this rejection.

Claim 1 recites a CMOS image sensor circuit comprising, *inter alia*, a chip including an "image sensor portion having a first area and a second area." The chip is formed to have "at least a first set of parallel edges including a first edge and a second edge," and "a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge." The image sensor portion includes "imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said chip," and "imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said chip."

Schick et al. discloses an "ordinary" CMOS active pixel device 101 in FIG. 1, as discussed in col. 5, beginning at line 14. Pixel device 101 has the unitary active area 102, and the inactive area 103. FIG. 2 of Schick et al. illustrates pixel device 200 which contains the unitary "large rectangular active area 201." The thin, non-active area 202 is

shifted away from the edge of the chip to allow room for the "substrate bonding area 203." Schick et al. does not teach or suggest a CMOS image sensor having a chip with "an image sensor portion having a first area and a second area."

Applicants respectfully urge that the explanation in the Office Action for the alleged teaching by Schick et al. of an image sensor portion having a first image area and a second area is untenable. The image sensor portion is described on page 3 of the Office Action as having "a first area" and "a second area." Two different explanations of the "first area" and the "second area" appear in the first and third paragraphs on page 3 of the Office Action. These two descriptions are contradictory, however, and do not properly track the language of the present claims.

As described in the first paragraph on page 3 of the Office Action, the first area is "one side of the column drive transistors which have been moved away from the edge." As shown in FIG. 2A and described by Schick et al., the column drive transistors are located in inactive area 202, making the first area the active area 201 shown in FIG. 2A of Schick et al. The second area is "on the other side of the column drive transistors," and thus corresponds to substrate bonding area 203. According to claim 1, though, each of the active layers contains imaging pixels. The substrate bonding area 203 of Schick et al. does not contain pixels, however, and consequently cannot be the second area of the active sensor portion.

Moreover, the Office Action states in the third paragraph on page 3 that imaging pixels of the first area of the image sensor portion are adjacent the first edge and the third edge of each chip, and imaging pixels of the second area of the image sensor portion are adjacent the second edge and the third edge of each chip. The Office Action references the top edge as shown in FIG. 2A as the first edge, with the second edge on the bottom, the third edge on the left, and the fourth edge on the right. The second area 203, however, which appears along the fourth edge, all the way to the right in FIG. 2A, cannot at the same time be adjacent the third edge all the way to the left in FIG. 2A.

Even if Schick et al. can somehow be interpreted to have first and second image sensor areas, Heller et al. does not cure the deficiencies of Schick et al. Heller et al. has been cited in an attempt to provide on-chip pixel interpolation, which the Office Action admits is missing from Schick et al. Heller et al. has a single sensor array 12, however, and so does not provide the missing feature of "an image sensor portion having a first area and a second area." Claim 1 is patentable over the proposed combination of Schick et al. and Heller et al. Claims 2-7 and 19-21 depend directly or indirectly from claim 1, and so are patentable for at least the same reasons.

Claim 8 recites a method of capturing an image comprising, *inter alia*, "providing at least two image sensor chips, each chip having first and second parallel edges," and "an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edge," and "includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges." The method also includes "abutting said image sensor chips along at least one of corresponding first and second edges."

Schick et al. discloses a method of capturing an image by providing two image sensor chips each having first and second parallel edges. Schick et al. does not teach or suggest capturing an image by providing two such image sensor chips with "a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges."

Heller et al. does not cure the deficiencies of Schick et al. The sensor array disclosed by Heller et al. has an undivided sensor array with control logic located on the chip outside the array. Applicants note that the text on the bottom of page 3 of the Office Action appears to end abruptly, and an explanation of the rejection of claim 8 was not found. Claim 8 is patentable over the proposed combination of Schick et al. and Heller et al.

Claim 9 recites a CMOS imager comprising, *inter alia*, a first CMOS image sensor chip having "a control portion and a centralized row-local control portion." The centralized row-local control portion is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said CMOS image sensor portion," and thereby forms "at least two image sensor areas." As noted above with respect to claim 1, Schick et al. does not teach or suggest an image sensor portion with "at least two image sensor areas." Heller et al., also having a monolithic image sensor portion, does not cure the deficiencies of Schick et al. Claim 9, and its dependent claim 10, are patentable over the proposed combination of Schick et al. and Heller et al.

Claim 11 recites a method of making a CMOS imager comprising, *inter alia*, "fabricating at least two CMOS image sensor chips having an image sensor portion arranged in an array of rows and columns," "each having a control portion and a centralized row-local control portion," with "said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array formed on said image sensor chip," and "thereby forming at least two image sensor areas for each of said at least two CMOS image sensor chips." As noted above in connection with claims 1 and 9, Schick et al. does not teach or suggest an image sensor portion made with "at least two image sensor areas." Heller et al., also having a monolithic image sensor portion, does not cure the deficiencies of Schick et al. Claim 11, and its dependent claim 12, are patentable over the proposed combination of Schick et al. and Heller et al.

Claim 13 recites an image sensor circuit having, *inter alia*, two image sensor chips, each chip having "an image sensor portion having a first area and a second area." As noted above in connection with claims 1, 9, and 11, Schick et al. does not teach or suggest an image sensor portion made with "a first area and a second area." Heller et al. also has a monolithic image sensor portion, and does not cure the deficiencies of Schick et al. Claim 13 is patentable over the proposed combination of Schick et al. and Heller et al.

Claim 17 recites a method of fabricating a CMOS imager that includes, *inter alia*, "forming at least two active image sensor areas in each of said at least two CMOS image sensor chips." Schick et al. does not teach or suggest fabricating a CMOS imager by forming CMOS image sensor chips with "at least two active image sensor areas" as recited in claim 17. Heller et al. also has a monolithic image sensor portion, and does not cure the deficiencies of Schick et al. Claim 17 is patentable over the proposed combination of Schick et al. and Heller et al.

Claims 5 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Heller et al., further in view of U.S. Pat. No. 5,886,353 to Spivey et al. Applicants respectfully request reconsideration of this rejection.

Claim 5 depends from claim 1, which is patentable over the Schick et al. in view of Heller et al. Spivey et al. has not been cited against claim 1. Even if properly cited against claim 1, Spivey et al. would not cure the deficiencies of Schick et al. in view of Heller et al. Spivey et al. has been cited as providing interpolation, as noted above. Spivey et al. has a unitary imager portion, and so does not provide the teachings of "a first area and a second area" in the imager portion. Claim 1, and its dependent claims 2-7 and 19-21, are patentable over the proposed combination of Schick et al., Heller et al., and Spivey et al.

Claim 12 depends from claim 11. Claim 11 is patentable over Schick et al. in view of Heller et al. Spivey et al. has not been cited against claim 11. Even if properly cited, Spivey et al. would not cure the deficiencies of Schick et al. in view of Heller et al. Spivey et al. has been cited as providing interpolation of pixels caused by row select logic and spaces between pixel pitches. Spivey et al. has a unitary imager portion, and does not provide the missing teachings of an image sensor portion made with "at least two image sensor areas." Claim 11, and its dependent claim 12, are patentable over the proposed combination of Schick et al., Heller et al., and Spivey et al.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Heller et al., further in view of U.S. Pat. No. 5,510,623 to Sayag et al. Applicants respectfully request reconsideration of this rejection.

Claim 6 depends from claim 1, which is patentable over Schick et al. in view of Heller et al. Sayag et al. has not been cited against claim 1, and even if it had been properly cited against claim 1, would not cure the deficiencies of Schick et al. in view of Heller et al. Sayag et al. has been cited as providing row logic in the center of the plurality of pixels. The proposed combination of Schick et al. with Sayag et al. would require modifying Schick et al. by placing an inactive area in the center of the active area. There is no motivation in the prior art for such a modification, however. Schick et al. discloses a large area imager in which the imager chips are arranged so that no light falls on any inactive areas. Consequently, it would be counterintuitive, at best, to modify Schick et al. by providing a central inactive area upon which light would strike. Schick et al. teaches directly away from providing a central inactive area, the motivation for which comes only from an improper attempt at hindsight reconstruction of applicants' invention. Claim 1, and its dependent claims 2-7 and 19-21, are patentable over the proposed combination of Schick et al, Heller et al., and Sayag et al.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Heller et al., further in view of U.S. PG PUB 2002/0000549 in the name of Spartiotis et al. Applicants respectfully request reconsideration of this rejection.

Claim 7 depends from claim 1, which is patentable over Schick et al. in view of Heller et al. Spartiotis et al. has not been cited against claim 1. Even if Spartiotis et al. had been properly cited against claim 1, it would not cure the deficiencies of Schick et al. in view of Heller et al. Spartiotis et al. has been cited as providing a guard ring. Spartiotis et al. does not provide the missing "image sensor portion having a first area and a second area," for example. Claim 1, and its dependent claims 2-7 and 19-21, are patentable over Schick et al., in view of Heller et al., further in view of Spartiotis et al.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Schick et al. in view of Spivey et al. Applicants respectfully request reconsideration of this rejection.

Claim 8 recites a method of capturing an image comprising, *inter alia*, "providing at least two image sensor chips, each chip having first and second parallel edges," and "an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edge," and "includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges." The method also includes "abutting said image sensor chips along at least one of corresponding first and second edges."

Schick et al. discloses a method of capturing an image by providing two image sensor chips each having first and second parallel edges. Schick et al. does not teach or suggest capturing an image by providing two such image sensor chips with "a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges." Spivey et al. does not cure the deficiencies of Schick et al. Spivey et al. has been cited as providing interpolation that is missing from Schick et al. Spivey et al. discloses overlapping imager chips along lines similar to the chip arrangement in Schick et al. The chips in both patents are overlapped such that light does is blocked by active areas from impacting the inactive areas. Schick et al. and Spivey et al. teach directly away from including an inactive area centrally in the image sensor array. Claim 8 is patentable over the cited references to Schick et al. and Spivey et al.

In view of the above amendment, applicants believe the pending application is in condition for allowance.

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